

2811

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Applicant(s): **Divakaruni et al.**

Docket No.

**BUR920000016US1**

Serial No.

**09/718,850**

Filing Date

**November 22, 2000**

Examiner

**G. Munson**

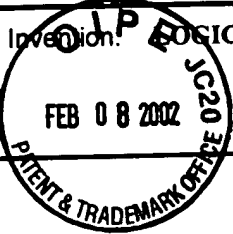
Group Art Unit

**2811**

Invention: **LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR**

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I hereby certify that this **RESPONSE TO RESTRICTION REQUIREMENT**  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Divakaruni, et al

Serial No.: 09/718,850

Filed: November 22, 2000

For: LOGIC SOI STRUCTURE, PROCESS AND  
APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

Honorable Assistant Commissioner of Patents  
Washington, D.C. 20231



Group Art Unit: 2811

Examiner: G. Munson

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**RESPONSE TO RESTRICTION REQUIREMENT**

Sir:

In response to the Office Action dated January 3, 2002, please consider the following:

**REMARKS**

In response to the Restriction Requirement, Applicants hereby elect the invention of Group II, (Claims 1-17), without traverse. Applicants reserve the opportunity to file a Divisional Application for the non-elected invention later. Early, favorable prosecution on the merits is respectfully requested.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.